ECR #: 11
Title: PCI Target Latency Exception
Release Date: Feb. 10, 1997
Impact: Change
Spec Version: A.G.P. 1.0

Summary

This ECR grants an exception to the PCI 2.1 target subsequent latency rule for A.G.P. compliant targets, to allow for improved performance.

Background:

Since A.G.P. is a point to point connection the need to adhere to the PCI subsequent latency requirement is not critical and in some cases may actually cause a performance degradation. Since only the corelogic and the A.G.P. compliant master are involved in the transaction, the insertion of additional waitstates may be better than terminating and re-initiating the transaction. The A.G.P. compliant target has all the information needed to determine when performance can be improved by inserting more than 8 waitstates on a subsequent data phase.

Change Current Specification as shown:

Change the footnote #4 on page 9, section 3.1 as follows:

4) The A.G.P. Compliant Target must behave as a PCI 2.1 compliant Master and Target with one exception. The A.G.P. Compliant Target is not required to adhere to either the target initial latency requirements or the target subsequent latency requirements as stated in the PCI 2.1 specification.